

Abstract of the Disclosure

A duty cycle correction circuit and a delay locked loop (DLL) including the duty cycle correction circuit, are capable of controlling their operation in order to correctly analyze the cause of generation of a duty cycle error when the duty cycle error is generated in the DLL. The duty cycle correction circuit selectively outputs to a DLL core duty cycle offset information for controlling a duty cycle of an internal clock signal synchronized to an external clock signal under the control of a switching control signal. The DLL corrects the duty cycle of a reference clock signal according to the duty cycle offset information, thereby outputting a reference clock signal having a 50% duty cycle.